**Amendments to the Claims**:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-9 (canceled)

10. (currently amended) ~~The circuit of claim 9 further comprising:~~ A circuit comprising:

a first transistor having a control terminal, an input terminal, and an output terminal, wherein said first transistor control terminal is coupled to a first feedback control block output and said first transistor input terminal is coupled to receive a positive supply voltage;

a second transistor having a control terminal, an input terminal, and an output terminal, wherein said second transistor control terminal is coupled to receive a data signal and said second transistor input terminal is coupled to said first transistor output terminal;

a third transistor having a control terminal, an input terminal, and an output terminal, wherein said third transistor control terminal is coupled to receive said data signal and said third transistor output terminal is coupled to said second transistor output terminal;

a fourth transistor having a control terminal, an input terminal, and an output terminal, wherein said fourth transistor control terminal is coupled to a second feedback control block output, said fourth transistor output terminal is coupled to said third transistor input terminal, and said fourth transistor input terminal is coupled to receive a supply voltage less positive than said positive supply voltage;

a first feedback control block having an input and said first feedback control block output, wherein said first feedback control block input is coupled to said second transistor output terminal;

a second feedback control block having an input and said second feedback control block output, wherein said second feedback control block input is coupled to said third transistor output terminal; and

a fifth transistor having a control terminal, an input terminal, and an output terminal, wherein said fifth transistor control terminal is coupled to receive said data signal, said fifth transistor input terminal is coupled to receive said positive supply voltage, and said fifth transistor output terminal is coupled to said second transistor output terminal.

11. (currently amended) ~~The circuit of claim 9 further comprising:~~ A circuit comprising:

a first transistor having a control terminal, an input terminal, and an output terminal, wherein said first transistor control terminal is coupled to a first feedback control block output and said first transistor input terminal is coupled to receive a positive supply voltage;

a second transistor having a control terminal, an input terminal, and an output terminal, wherein said second transistor control terminal is coupled to receive a data signal and said second transistor input terminal is coupled to said first transistor output terminal;

a third transistor having a control terminal, an input terminal, and an output terminal, wherein said third transistor control terminal is coupled to receive said data signal and said third transistor output terminal is coupled to said second transistor output terminal;

a fourth transistor having a control terminal, an input terminal, and an output terminal, wherein said fourth transistor control terminal is coupled to a second feedback control block output, said fourth transistor output terminal is coupled to said third transistor input terminal, and said fourth transistor input terminal is coupled to receive a supply voltage less positive than said positive supply voltage;

a first feedback control block having an input and said first feedback control block output, wherein said first feedback control block input is coupled to said second transistor output terminal;

a second feedback control block having an input and said second feedback control block output, wherein said second feedback control block input is coupled to said third transistor output terminal; and

a sixth transistor having a control terminal, an input terminal, and an output terminal, wherein said sixth transistor control terminal is coupled to receive said data signal, said sixth transistor input terminal is coupled to receive said supply voltage less positive than said positive supply voltage, and said sixth transistor output terminal is coupled to said third transistor output terminal.

12. (currently amended) ~~The circuit of claim 9 further comprising:~~ A circuit comprising:

a first transistor having a control terminal, an input terminal, and an output terminal, wherein said first transistor control terminal is coupled to a first feedback control block output and said first transistor input terminal is coupled to receive a positive supply voltage;

a second transistor having a control terminal, an input terminal, and an output terminal, wherein said second transistor control terminal is coupled to receive a data signal and said second transistor input terminal is coupled to said first transistor output terminal;

a third transistor having a control terminal, an input terminal, and an output terminal, wherein said third transistor control terminal is coupled to receive said data signal and said third transistor output terminal is coupled to said second transistor output terminal;

a fourth transistor having a control terminal, an input terminal, and an output terminal, wherein said fourth transistor control terminal is coupled to a second feedback control block output, said fourth transistor output terminal is coupled to said third transistor input terminal, and said fourth transistor input terminal is coupled to receive a supply voltage less positive than said positive supply voltage;

a first feedback control block having an input and said first feedback control block output, wherein said first feedback control block input is coupled to said second transistor output terminal;

a second feedback control block having an input and said second feedback control block output, wherein said second feedback control block input is coupled to said third transistor output terminal;

a fifth transistor having a control terminal, an input terminal, and an output terminal, wherein said fifth transistor control terminal is coupled to receive said data signal, said fifth transistor input terminal is coupled to receive said positive supply voltage, and said fifth transistor output terminal is coupled to said second transistor output terminal; and

a sixth transistor having a control terminal, an input terminal, and an output terminal, wherein said sixth transistor control terminal is coupled to receive said data signal, said sixth transistor input terminal is coupled to receive said supply voltage less positive than said positive supply voltage, and said sixth transistor output terminal is coupled to said third transistor output terminal.

13. (currently amended) ~~The circuit of claim 9~~ A circuit comprising:

a first transistor having a control terminal, an input terminal, and an output terminal, wherein said first transistor control terminal is coupled to a first feedback control block output and said first transistor input terminal is coupled to receive a positive supply voltage;

a second transistor having a control terminal, an input terminal, and an output terminal, wherein said second transistor control terminal is coupled to receive a data signal and said second transistor input terminal is coupled to said first transistor output terminal;

a third transistor having a control terminal, an input terminal, and an output terminal, wherein said third transistor control terminal is coupled to receive said data signal and said third transistor output terminal is coupled to said second transistor output terminal;

a fourth transistor having a control terminal, an input terminal, and an output terminal, wherein said fourth transistor control terminal is coupled to a second feedback control block output, said fourth transistor output terminal is coupled to said third transistor input terminal, and said fourth transistor input terminal is coupled to receive a supply voltage less positive than said positive supply voltage;

a first feedback control block having an input and said first feedback control block output, wherein said first feedback control block input is coupled to said second transistor output terminal;

a second feedback control block having an input and said second feedback control block output, wherein said second feedback control block input is coupled to said third transistor output terminal; and

wherein said first feedback control block comprises a transmission gate.

14. (currently amended) ~~The circuit of claim 9~~ A circuit comprising:

a first transistor having a control terminal, an input terminal, and an output terminal, wherein said first transistor control terminal is coupled to a first feedback control block output and said first transistor input terminal is coupled to receive a positive supply voltage;

a second transistor having a control terminal, an input terminal, and an output terminal, wherein said second transistor control terminal is coupled to receive a data signal and said second transistor input terminal is coupled to said first transistor output terminal;

a third transistor having a control terminal, an input terminal, and an output terminal, wherein said third transistor control terminal is coupled to receive said data signal and said third transistor output terminal is coupled to said second transistor output terminal;

a fourth transistor having a control terminal, an input terminal, and an output terminal, wherein said fourth transistor control terminal is coupled to a second feedback control block output, said fourth transistor output terminal is coupled to said third transistor input terminal, and said fourth transistor input terminal is coupled to receive a supply voltage less positive than said positive supply voltage;

a first feedback control block having an input and said first feedback control block output, wherein said first feedback control block input is coupled to said second transistor output terminal;

a second feedback control block having an input and said second feedback control block output, wherein said second feedback control block input is coupled to said third transistor output terminal; and

wherein said second feedback control block comprises a transmission gate.

Claims 15-30 (cancelled)